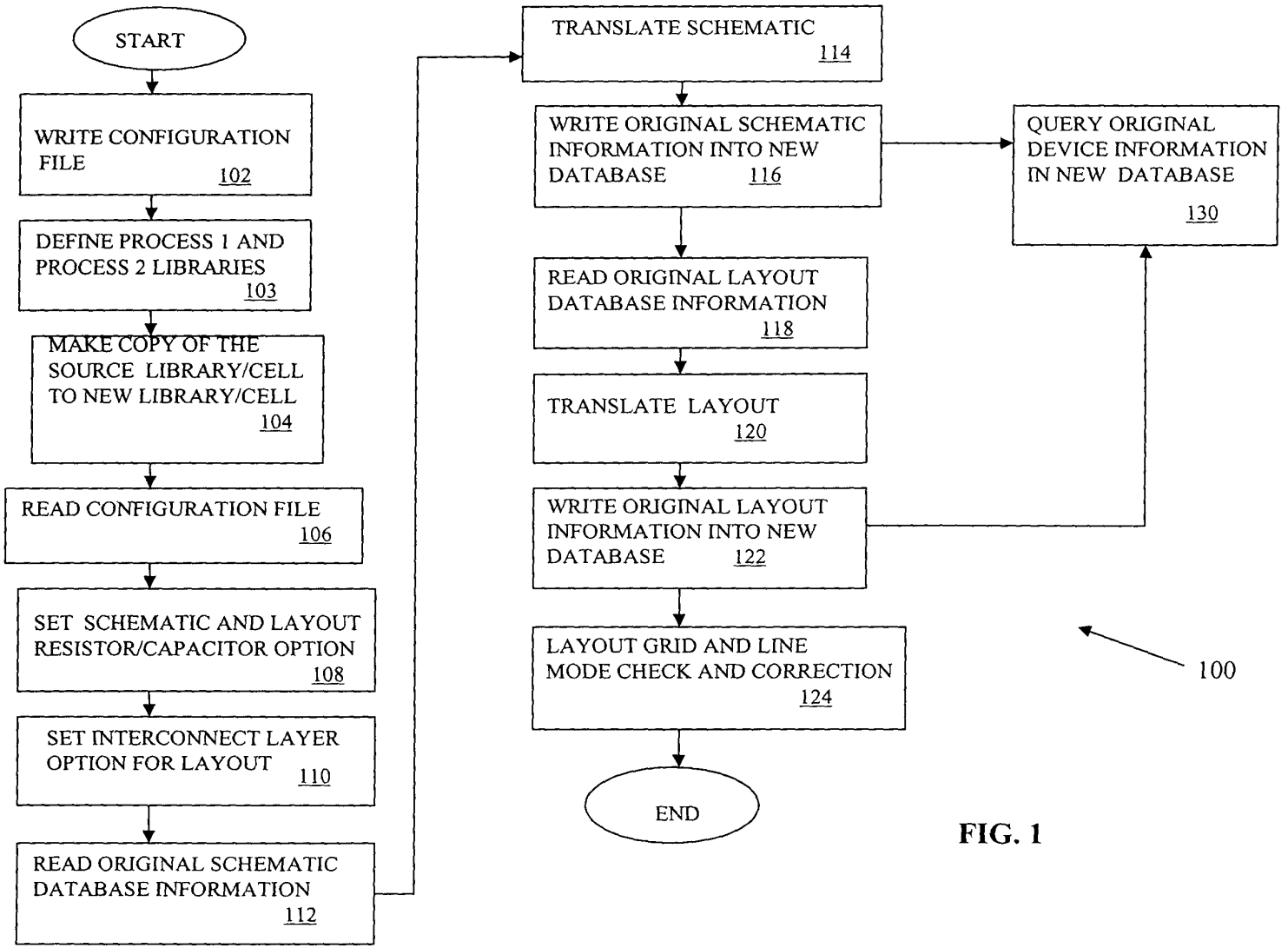

START
WRITE CONFIGURATION FILE 102
DEFINE PROCESS 1 AND PROCESS 2 LIBRARIES 103
MAKE COPY OF THE SOURCE LIBRARY/CELL TO NEW LIBRARY/CELL 104
READ CONFIGURATION FILE 106
SET SCHEMATIC AND LAYOUT RESISTOR/CAPACITOR OPTION 108
SET INTERCONNECT LAYER OPTION FOR LAYOUT 110
READ ORIGINAL SCHEMATIC DATABASE INFORMATION 112
TRANSLATE SCHEMATIC 114
WRITE ORIGINAL SCHEMATIC INFORMATION INTO NEW DATABASE 116
QUERY ORIGINAL DEVICE INFORMATION IN NEW DATABASE 130
READ ORIGINAL LAYOUT DATABASE INFORMATION 118
TRANSLATE LAYOUT 120
WRITE ORIGINAL LAYOUT INFORMATION INTO NEW DATABASE 122
LAYOUT GRID AND LINE MODE CHECK AND CORRECTION 124
END
100

FIG. 1

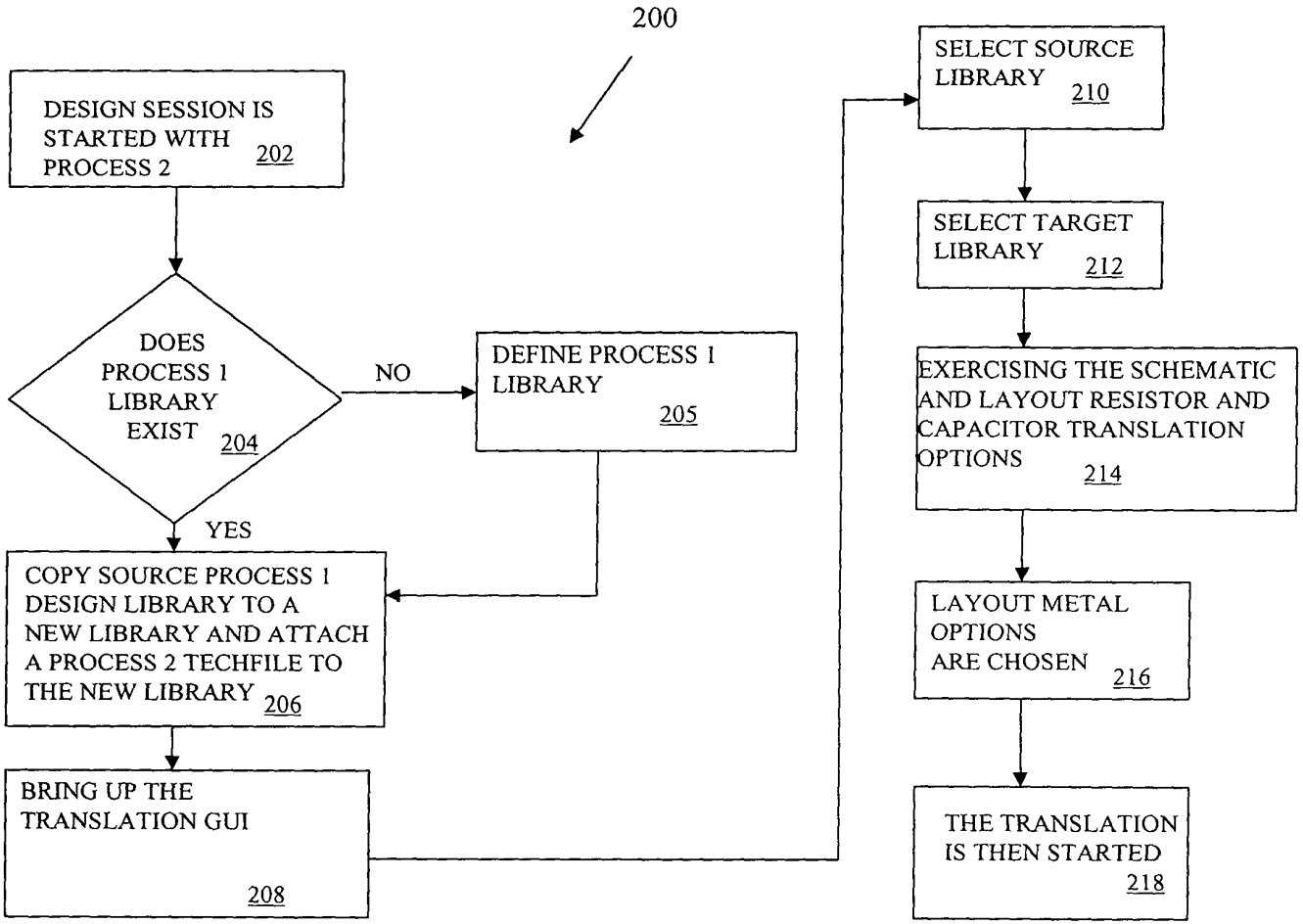

200
DESIGN SESSION IS STARTED WITH PROCESS 2 202
DOES PROCESS 1 LIBRARY EXIST 204
NO
DEFINE PROCESS 1 LIBRARY 205
YES
COPY SOURCE PROCESS 1 DESIGN LIBRARY TO A NEW LIBRARY AND ATTACH A PROCESS 2 TECHFILE TO THE NEW LIBRARY 206
BRING UP THE TRANSLATION GUI 208
SELECT SOURCE LIBRARY 210
SELECT TARGET LIBRARY 212
EXERCISING THE SCHEMATIC AND LAYOUT RESISTOR AND CAPACITOR TRANSLATION OPTIONS 214
LAYOUT METAL OPTIONS ARE CHOSEN 216
THE TRANSLATION IS THEN STARTED 218

FIG. 2

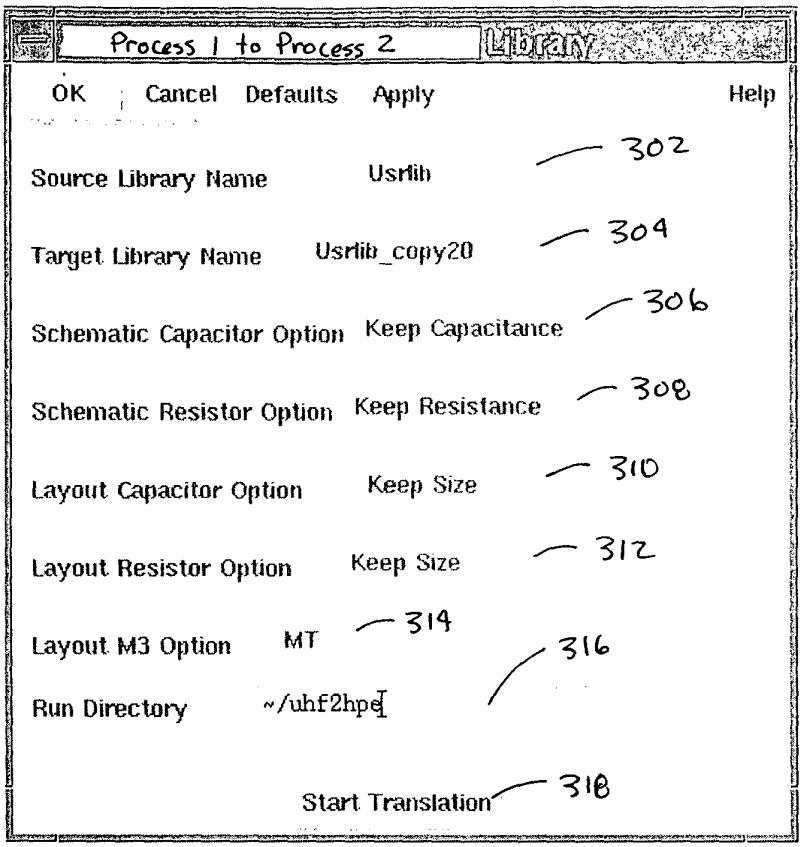

Process 1 to Process 2
Library
OK
Cancel
Defaults
Apply
Help
Source Library Name
Usrlib
Target Library Name
Usrlib_copy20
Schematic Capacitor Option
Keep Capacitance
Schematic Resistor Option
Keep Resistance
Layout Capacitor Option
Keep Size
Layout Resistor Option
Keep Size
Layout M3 Option
MT
Run Directory
~/uhf2hpe
Start Translation
300
302
304
306
308
310
312
314
316
318

FIG.3

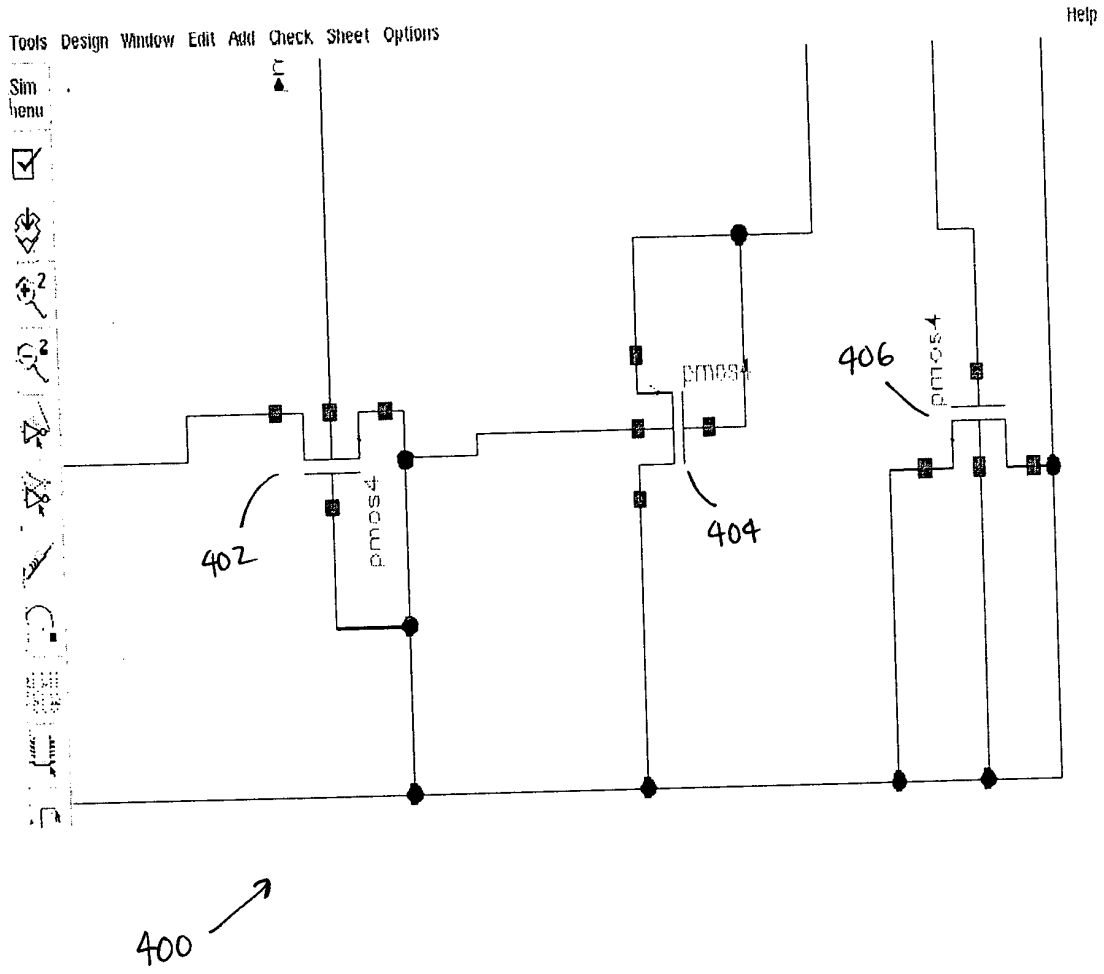

Tools Design Window Edit Add Check Sheet Options
Help
Sim
Menu
pmos4
pmos4
pmos4
402
404
406
400

FIG. 4

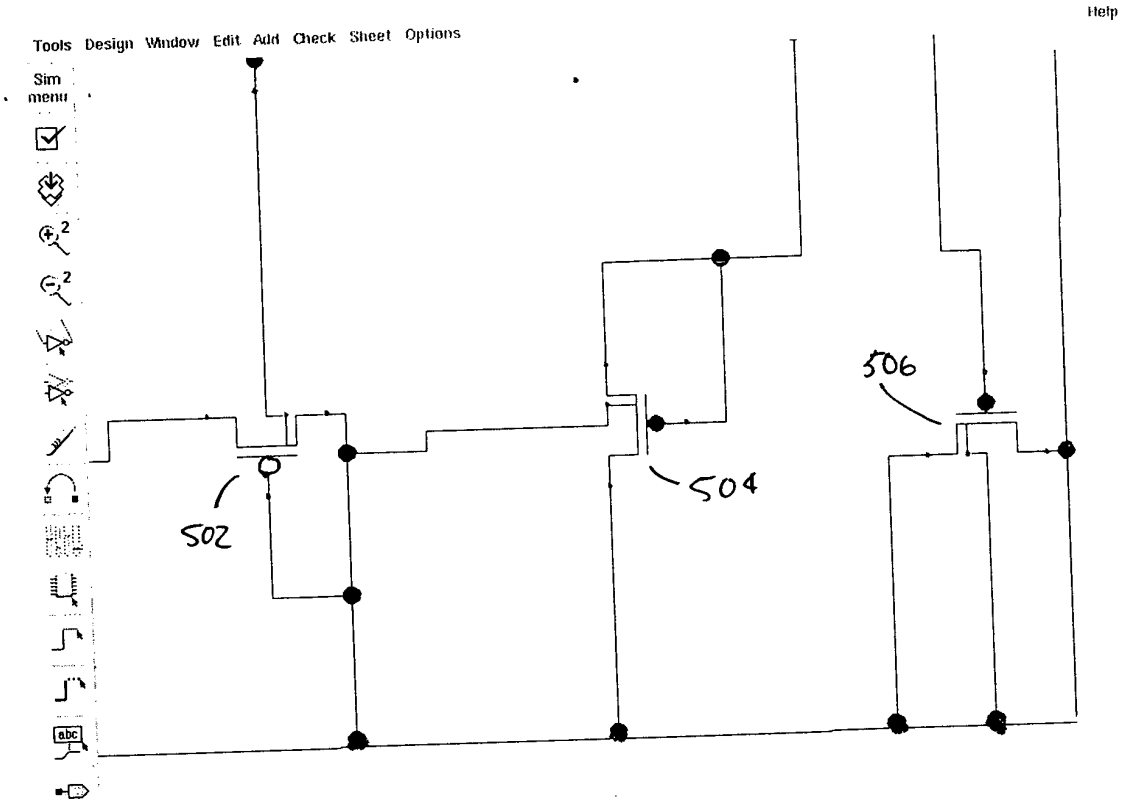

Tools Design Window Edit Add Check Sheet Options
Help
Sim menu
502
504
506

FIG. 5

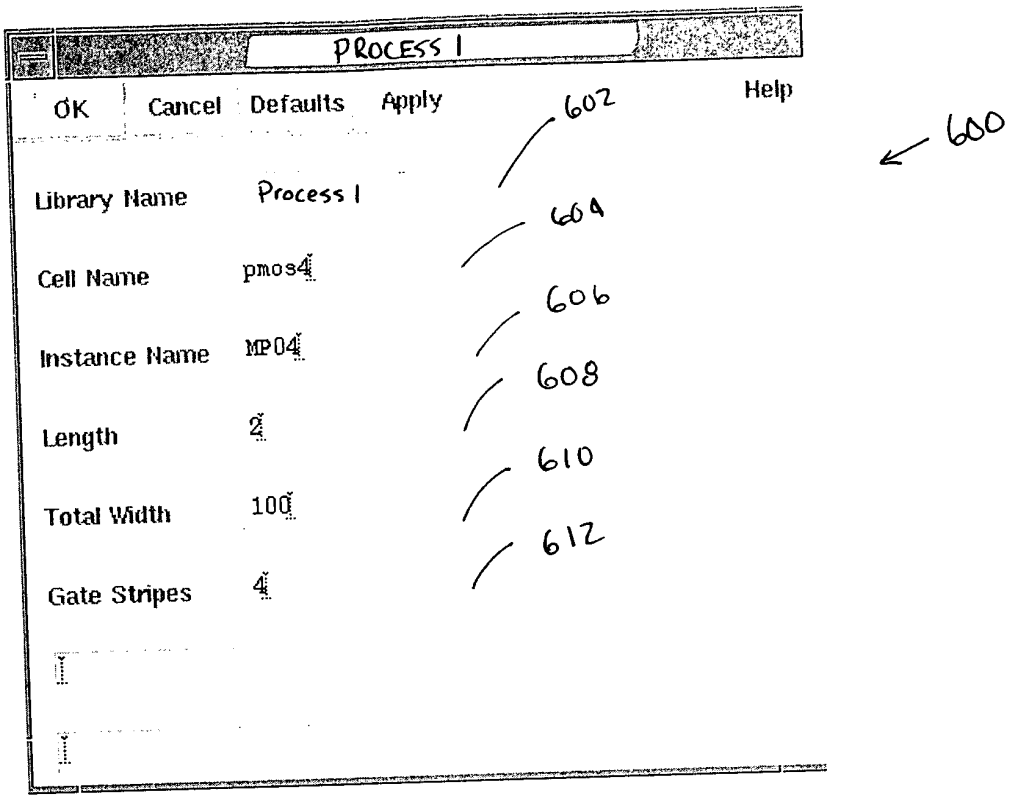

PROCESS 1
OK
Cancel
Defaults
Apply
Help
602
600
Library Name
Process 1
604
Cell Name
pmos4
606
Instance Name
MP04
608
Length
2
610
Total Width
100
612
Gate Stripes
4

FIG. 6

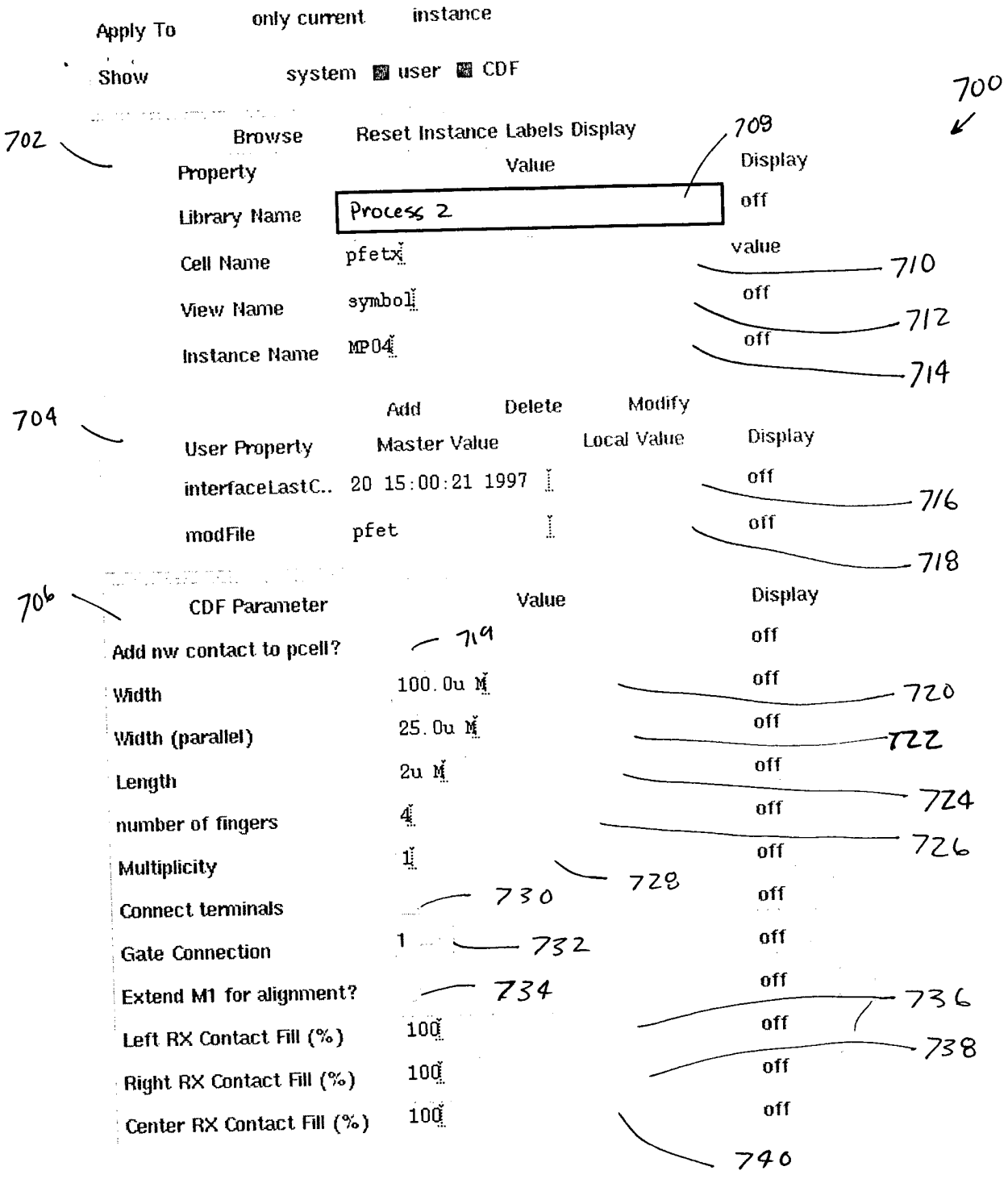

Apply To only current instance
Show system user CDF
700
Browse
Reset Instance Labels Display
702
708
Property
Value
Display
Library Name
Process 2
off
Cell Name
pfetx
value
710
View Name
symbol
off
712
Instance Name
MP04
off
714
Add
Delete
Modify
704
User Property
Master Value
Local Value
Display
interfaceLastC..
20 15:00:21 1997
off
716
modFile
pfet
off
718
706
CDF Parameter
Value
Display
Add nw contact to pcell?
719
off
Width
100.0u M
off
720
Width (parallel)
25.0u M
off
722
Length
2u M
off
724
number of fingers
4
off
726
Multiplicity
1
728
off
Connect terminals
730
off
Gate Connection
1
732
off
Extend M1 for alignment?
734
off
736
Left RX Contact Fill (%)
100
off
738
Right RX Contact Fill (%)
100
off
Center RX Contact Fill (%)
100
off
740

FIG. 7

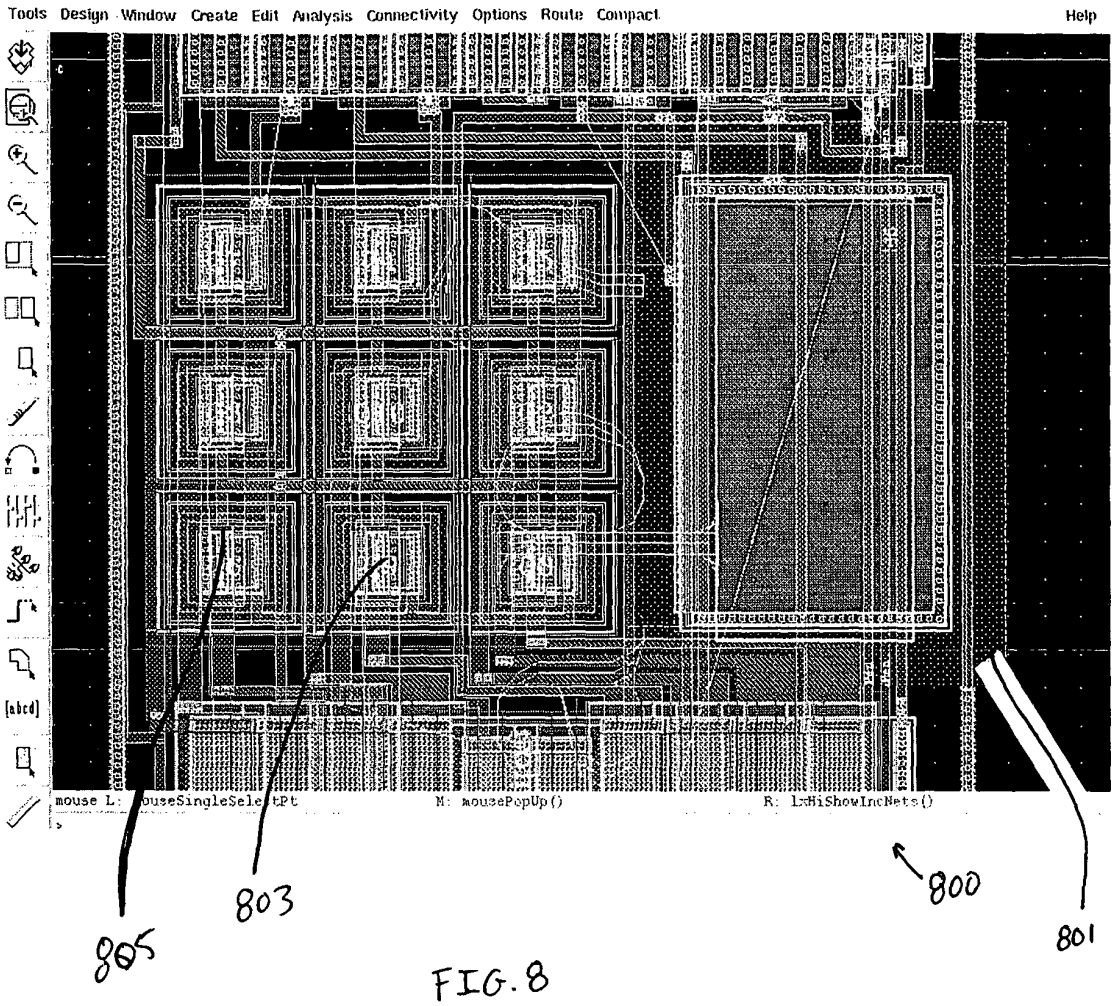

Tools Design Window Create Edit Analysis Connectivity Options Route Compact Help
[abcd]
mouse L: ouseSingleSele tPt
M: mousePopUp()
R: lxHiShowInetNets()
805
803
800
801

FIG. 8

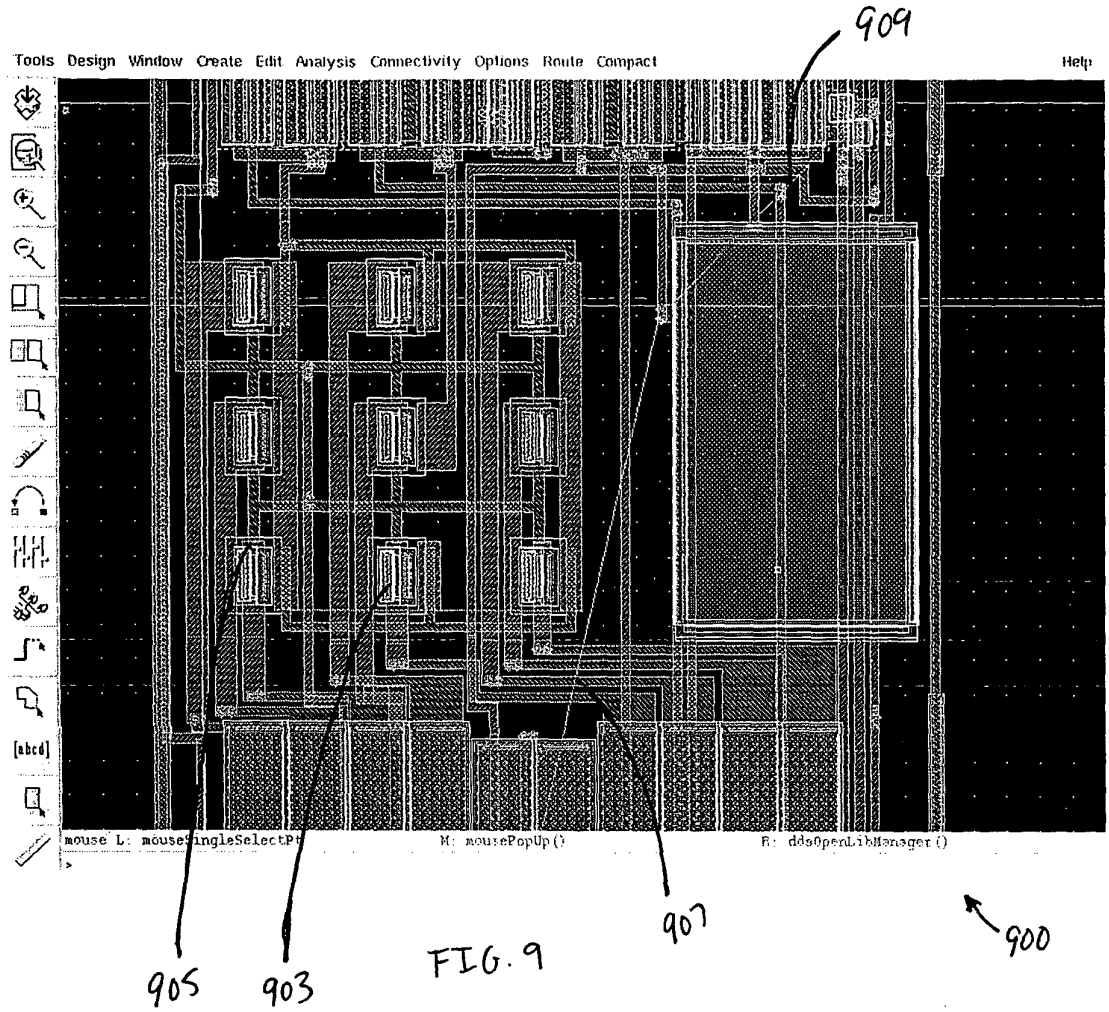


FIG. 9

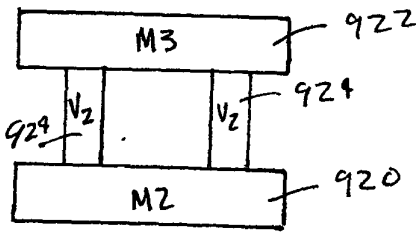


FIG. 9A

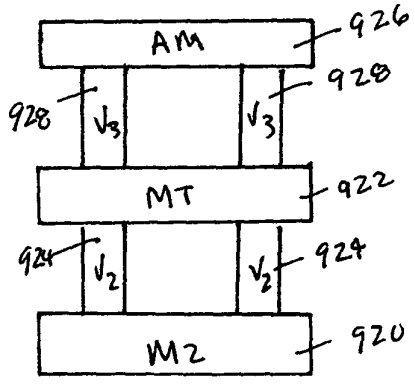
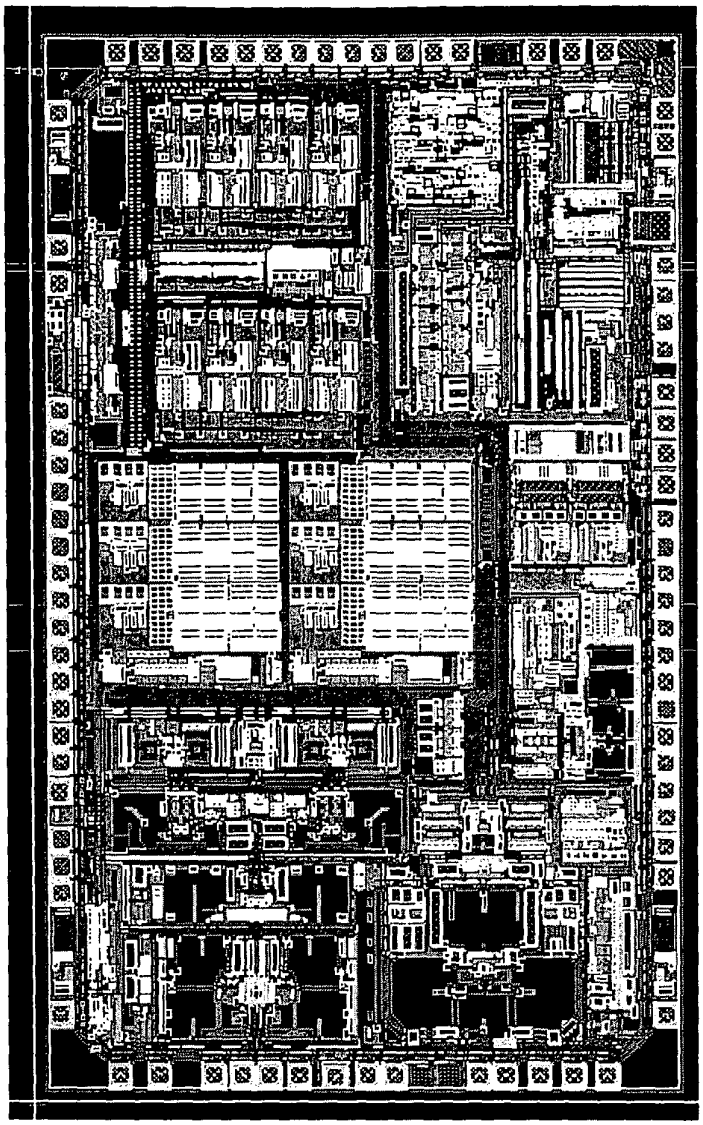


FIG. 9B



1000

FIG. 10